WHAT IS CLAIMED IS:

1. A compiler type simulator for software development, said compiler type simulator comprising:

a compiler operable to compile a source code described in a high-level language; and

a library including at least one of a plurality of functions and a plurality of procedures that are defined in the high-level language and model components of a target processor different from a host processor,

wherein the source code is described using said library.

2. The compiler type simulator as recited in claim 1, wherein the components of the target processor comprise:

an accumulator of the target processor;

a memory controller of the target processor; and

a register of the target processor.

3. The compiler type simulator as recited in claim 1, wherein said library comprises:

a hardware model library defining in the high-level language the at least one of the plurality of functions and the plurality of procedures that model the components of the target processor; and

an instruction-set-library defining in the high-level language at least one of a plurality of functions and a plurality of procedures corresponding to instructions of the target processor using the at least one of the plurality of functions and the plurality of procedures of said hardware model library.

4. The compiler type simulator as recited in claim 3, wherein the instructions of the target processor comprise an ADD instruction, an SUB instruction, an AND instruction, an OR instruction, an LD instruction, an ST instruction, an SET instruction and an MOV instruction.

5. The compiler type simulator as recited in claim 1, wherein the at least one of the plurality of functions and the plurality of procedures of said library comprises a function and a procedure operable to calculate at least one of

an executing-cycles-number of the target processor

and

power consumption of the target processor.

6. The compiler type simulator as recited in claim 1, wherein at least one of

an executing-cycles-number of the target processor

and

power consumption of the target processor

can be changed.

7. The compiler type simulator as recited in claim 1, wherein the at least one of the plurality of functions and the plurality of procedures of said library comprises a function and a procedure operable to calculate code size in the target processor.

8. An interpreter type simulator for software development, said interpreter type simulator comprising:

a translator operable to read a source code described in a high-level language to output an object-code;

an instruction-fetching unit operable to fetch the object-code to output a fetched object-code;

an instruction-decoding unit operable to decode the fetched object-code to output a decoded object-code;

an executing unit operable to execute the decoded object-code; and

a library including at least one of a plurality of functions and a plurality of procedures that are defined in the high-level language and model components of a target processor different from a host processor,

wherein the source code is described using said library.

9. A simulation program recorded on a recoding medium, said simulation program comprising:

a compiler operable to compile a source code described in a high-level language; and

a library including at least one of a plurality of functions and a plurality of procedures that are defined in the high-level language and model components of a target processor different from a host processor,

wherein the source code is described using said library.